62.(New) The capacitor of claim 61 wherein:

the conductive layer comprises polysilicon; and

the capacitor further comprises a source/drain diffusion in the substrate.

63.(New) A capacitor comprising:

a first polysilicon layer supported by a substrate;

a layer of amorphous carburized silicon in contact with the first polysilicon layer; and

a second polysilicon layer in contact with the layer of amorphous carburized silicon.

64.(New) The capacitor of claim 63, further comprising a source/drain diffusion in the substrate.

REMARKS

In response to the Office Action mailed November 23, 1999, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 1-6 and 20-38 are pending in the application, and are rejected. Claim 38 has been amended to correct for antecedent basis only, and was not amended in response to the rejection of the claims. Claims 39-64 have been added. No new matter has been added.

Information Disclosure Statement

Applicant submitted a Supplemental Information Disclosure Statement on November 22, 1999. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant further requests that a copy of the form 1449, initialed by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Double Patenting

The Examiner provisionally rejected claims 1-6 under the judicially created doctrine of obviousness-type double patenting over claims 11-18 of copending Application Serial No. 08/902,843. The applicant will address this issue when pending claims in Application Serial No. 08/902,843 are indicated as allowable and the pending claims in the above-identified application are otherwise indicated as allowable.

Rejection of the Claims under 35 USC § 102(b)

Claims 4, 5, 20, 23, 29, 32, and 36 were rejected under 35 USC § 102(b) as being anticipated by Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata). The applicant respectfully traverses.

Claim 20 recites a memory cell comprising a floating gate and a layer of amorphous carburized silicon between the floating gate and a substrate.

Sakata does not disclose a gate. Sakata discloses in Figure 1 a diode structure comprising c-Si, a layer of hydrogenated amorphous silicon carbide (a-SiC:H), a layer of hydrogenated amorphous silicon (a-Si:H), another layer of a-SiC:H, and Al. Column 3. Both a-SiC:H and a-Si:H are highly resistive, insulating layers. Both are hydrogenated to ensure high resistivity. A plot of capacitance-voltage (C-V) characteristics for the diode is shown in Fig. 2 of Sakata. The plot shows that the "capacitance at 3V (470pF) is in fairly good agreement with the calculated capacitance of stacked insulator layers." Column 2.

A gate is known to those skilled in the art as a continuous, electrically conductive structure. Sakata is disclosing a diode structure comprised entirely of "stacked insulator layers", and does not disclose a continuous, electrically conductive structure.

Sakata discloses that both electrons and holes "can be stored in the a-Si:H layer because of the discontinuity of the conduction (valence) band edges at the a-SiC:H/a-Si:H interfaces." Column 1. However, Sakata has not substantially identified the mechanism for the charge storage: "We speculate that traps in the a-Si:H and/or at the interface between a-Si:H and a-SiC:H are acting as memory sites." Column 2. The band edges shown in Figure 1 are also pure speculation by Sakata: "However, we speculate that a band offset exists at both band edges in the present samples, as schematically shown in Fig. 1, because both electrons and holes are stored in the a-Si:H layer." Column 2. The storage mechanism in the diode structure disclosed by Sakata is a product of pure speculation, and therefore Sakata does not disclose a gate.

The C-V plot shows a "large hysteresis" that may be used as a memory window. Column 2. While the hysteresis may be used to create a memory device, this does not imply that the diode structure has a gate. The diode structure of Sakata is comprised entirely of alternate layers of highly resistive insulators, and does not include a gate.

The applicant respectfully submits that Sakata does not disclose all the elements recited in claim 20, such as the floating gate, that claim 20 is not anticipated by Sakata, and that claim 20 is in condition for allowance.

Claims 4, 5, 23, 29, 32, and 36 recite limitations similar to those recited in claim 20. For reasons analogous to those stated above with respect to claim 20, and the limitations in the claims, that applicant respectfully submits that claims 4, 5, 23, 29, 32, and 36 are not anticipated by Sakata, and that these claims are in condition for allowance.

Rejection of the Claims under 35 USC § 103(a)

Claims 1-3, 6, 21, 22, 24-30, 33-34, and 37 were rejected under 35 USC § 103(a) as being unpatentable over Sakata. The applicant respectfully traverses.

Claims 1-3, 6, 21, 22, 24-30, 33-34, and 37 recite elements similar to those recited above in claim 20.

There must be a showing of a "teaching or motivation to combine prior art references" to support a rejection under section 103 and "the showing must be clear and particular." *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Such a showing of a "teaching or motivation to combine" is necessary to avoid the use of hindsight when combining references under section 103. 50 USPQ2d at 1616-17.

As mentioned above, Sakata is deficient in that Sakata does not disclose a gate. The Examiner has not identified a suggestion in Sakata for the addition of a gate. In fact, the diode structure comprised entirely of alternate layers of highly resistive insulators functions without a gate according to Sakata. The Examiner also has not identified a second reference that suggests the use of a gate with the structure of Sakata.

The Examiner is correct, in that Sakata has disclosed that the diode structure shown in Figure 1 may be used in a memory device. Column 1. However, this does not serve as a suggestion for the addition of source, drain, and channel regions to the diode structure of Sakata.

Applicant respectfully submits that claims 1-3, 6, 21, 22, 24-30, 33-34, and 37 are not disclosed or suggested by Sakata, and that claims 1-3, 6, 21, 22, 24-30, 33-34, and 37 are in condition for allowance.

Claims 31, 35, and 38 were rejected under 35 USC § 103(a) as being unpatentable over Sakata in view of Sugita (JP Patent No. 08-255878). The applicant respectfully traverses.

Claims 31, 35, and 38 recite elements similar to those recited above in claim 20. As mentioned above, Sakata is deficient in that Sakata does not disclose a gate. Sugita discloses a traditional floating gate transistor with a floating gate separated from a silicon substrate by an insulator. However, there is no suggestion to combine Sakata and Sugita. Sakata has only speculated on the reasons for the performance of the disclosed diode structure. The operation of

a traditional floating gate transistor is well known. The Examiner has not identified a suggestion in either Sakata or Sugita for combining the two different structures.

The applicant respectfully submits that claims 31, 35, and 38 are not disclosed or suggested by the combination of Sakata and Sugita, and that claims 31, 35, and 38 are in condition for allowance.

New Claims

The applicant has added new claims 39-64, and respectfully submits that all of the new claims 39-64 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

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Date 16 FEB 2000 By _____

Robert E. Mates
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on **February 16, 2000**.

Susan Johnson
Name

Susan Johnson
Signature